WHAT IS CLAIMED IS:

1. A method of fabricating a FLASH memory device comprising:

forming trench device isolation layers on a substrate for defining a plurality of parallel first active regions, and forming a stack on the first active regions comprising a gate insulation pattern, a conductive pattern, and a hard mask pattern, wherein the stack comprises sidewalls aligned to sidewalls of the trench device isolation layers;

removing the hard mask pattern at regular intervals along each of the first active regions for exposing a top of the conductive pattern;

forming an oxide pattern on the top of the conductive pattern;

removing the hard mask pattern;

etching the conductive pattern using the oxide pattern as an etch mask for forming floating gate patterns disposed on each of the first active regions at regular intervals;

forming tunnel oxide layers on sidewalls of the floating gate patterns; and

forming a plurality of parallel control gate electrodes disposed on the floating gate patterns, crossing over the first active regions.

2. The method of claim 1, wherein forming the trench device isolation layers comprises;

stacking a gate insulation layer, a conductive layer and a hard mask

layer on a substrate;

patterning successively the hard mask layer, the conductive layer, the gate insulation layer and the substrate to form the stack including a plurality of parallel patterns comprising the gate insulation pattern, the conductive pattern and the hard mask pattern;

etching the substrate to define a plurality of parallel active regions comprising the plurality of parallel first active regions and a plurality of second active regions using the hard mask pattern as an etch mask; and

filling an insulation layer within regions between the plurality of parallel patterns for forming the trench device isolation layer.

3. The method of claim 1, wherein the top of the conductive pattern is lower than a top of the trench device isolation layer.

4. The method of claim 1, further comprising performing a thermal oxidation of the conductive pattern for forming an oxide pattern, wherein the conductive pattern is formed of polysilicon.

5. The method of claim 1, wherein the exposing the top of the conductive pattern comprises:

forming a photoresist pattern on an entire surface of the substrate, wherein the photoresist pattern includes a plurality of parallel openings that intersect the first active regions and expose the hard mask pattern and the

trench device isolation layer; and

etching the hard mask pattern using the photoresist pattern as an etch mask.

6. The method of claim 1 further comprising forming a plurality of shared source regions disposed parallel to word lines and connected to the first active regions thereunder, wherein a pair of word lines are disposed between the plurality of shared source regions.

7. The method of claim 1, wherein defining the plurality of first active regions further comprises forming a plurality of parallel second active regions crossing over the first active regions for forming a mesh with the stack.

8. The method of claim 7, wherein the exposing the top of the conductive pattern comprises:

forming a photoresist pattern including a plurality openings parallel to the plurality of second active regions on an entire surface of the substrate, wherein a pair of openings are disposed between adjacent second active regions; and

etching the hard mask pattern using the photoresist pattern as an etch mask for exposing two portions of the top of the conductive pattern over the first active region between intersections of the first and second active regions.

9. The method of claim 1, further comprising forming word lines on a portion of the floating gates and the first active regions.

10. A method of fabricating a FLASH memory device comprising:

providing, sequentially, a substrate, a gate insulation layer, and a conductive layer, a hard mask layer;

forming trench device isolation layers in the substrate defining a plurality of parallel first active regions and a plurality of second active regions, the first and second active regions comprising a gate insulation pattern, and a conductive pattern, a hard mask pattern;

exposing portions of a top of the conductive pattern along each of the first active regions;

forming an oxide pattern on the top of the conductive pattern;

removing the hard mask pattern;

etching the conductive pattern using the oxide pattern as an etch mask for forming floating gate patterns disposed on each of the first active regions at regular intervals;

forming a plurality of word lines crossing over the plurality of first active regions, wherein the word lines are disposed on a portion of the floating gate pattern and on a portion each of the plurality of first action regions adjacent to the floating gate pattern.

11. The method of claim 10, wherein a pair of word lines is

disposed between adjacent second active regions forming a mesh shaped active region.

12. The method of claim 11, further comprising:

forming a drain region in each of the plurality of first active regions between the word lines; and

forming a source region in each of the plurality of second active regions between the word lines.